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| 10/026,614 | 12/27/2001 | Masashi Naito | KOKUSAI 086 | 9114 |

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| EXAMINER | |
|---|---|
| WONG, LINDA | |
| **ART UNIT** | **PAPER NUMBER** |
| 2611 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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| 3 MONTHS | 03/21/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/026,614 | NAITO ET AL. | |
| | Examiner | Art Unit | |
| | Linda Wong | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on *20 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,5,7,9 and 13-20* is/are pending in the application.

4a) Of the above claim(s) *4,6,8,10-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,7,9 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## *Response to Arguments*

### *Claim Objections*

1. Due to the amendments to claims 5 and 17, the objections as stated in the office action mailed 10/17/2006 is withdrawn.

### *Prior Art Rejection*

2. Regarding the prior art rejection, the applicant's arguments filed 12/20/2006 have been fully considered but they are not persuasive.
3. Page 11-13 of the applicant's arguments under section "The Claimed Invention", the applicant contends the claimed invention differs from the conventional, wherein the applicant's invention differs from the convention method by reducing or lowering the sampling rate. IN the own words of the applicant, the applicant contends

> "Conventionally, it was necessary to use a high over sample rate for an equalized process. However, the present inventors recognized that, as long as a high over sample rate is adopted to the symbol synchronization, the operation speed can be reduced.
>
> Applicants also have recognized that those skilled in the art may consider that the equalization accuracy to the propagation properties deteriorates by reducing the sample rate.
>
> In other words, the claimed invention is opposite to the conventional common sense (i.e., contrary to the conventional wisdom) of "the higher the sampling rate the better the results".
>
> However, Applicants have found that, by following quickly the variation of the propagation properties and following the properties more quickly by inserting one or more symbols and short symbol patterns at a short interval (for example, 16 symbols), the equalization accuracy to the propagation properties can be

improved by reducing the sample rate. When the symbol patterns are received, it is necessary to reflect weights of the equalizer immediately and the present invention uses an algorithm having a quick response.

For example, independent claim 1 exemplarily defines an equalizer for equalizing a detection signal obtained by detecting a reception signal at an oversampling rate, the reception signal periodically including known symbol patterns made up of at least one symbol, the equalizer including symbol pattern synchronizing means for reproducing symbol timing by detecting the symbol patterns based on the reception signal at the oversampling rate, equalizing means for acquiring an equalized signal by multiplying signals extracted from the reception signal at predetermined intervals of n samples and, symbol pattern generating means for generating a reference signal equal to the symbol patterns, error calculating means for acquiring an equalization error by subtracting the equalized signal from the reference signal, and weight updating means for updating the weights based on the detection signal and the equalization error at the timing of the symbol patterns detected from the reception signal of the oversampling rate. Independent claims 3, 5, 7, and 9 define somewhat similar devices (and methods), according to the present invention.

As recited, for example, by independent claims 1 and 3, the equalizer of the claimed invention has the equalizing means which is operated at predetermined intervals of n samples, weight updating means which update a tap coefficient by the symbol timing detected from the oversampling rate and data decision means which decide data at the symbol timing detected from the oversampling rate. In other words, the processing after equalizing means (inclusive) can be operated with a low sampling rate by decimating data except for symbol timing.

Furthermore, some of the superior effects based on the low sampling rate according to the claimed invention are described on page 20, lines 1-5, page 24, lines 24-27, and page 25, lines 4-10. "

Limitation such as "the processing after equalizing means (inclusive) can be operated with a low sampling rate by decimating data except for symbol timing" is not recited in the limitations. Furthermore, the claimed limitation does not indicate an actual rate in which the sampler is sampling the input signal. The

examiner has reviewed highlighted limitations, as shown in the arguments, in the claim as such:

> The input signal is sampled at an oversampling rate, the equalizer multiples the signal extracted from the reception signal, wherein the signal extracted comprises samples within a predetermined interval. The number of samples and predetermined interval is determined by the oversampling rate.

Based on this interpretation, the examiner respectfully disagrees that Kokuryo in view of Adireddy et al fails to disclose the claimed limitation. To further explain, Kokuryo discloses an analog to digital converter in Fig. 1, label 3, wherein the rate at which the analog to digital converter samples the input signal would depend on the setting of the analog to digital converter. The sampled inputs, labels Ir and Qr, are inputted into a training signal synchronization detector, label 12, for detecting the symbol pattern as disclosed in paragraph 0085. The equalizer, label 14, receives Ir and Qr, which are buffered by memory blocks 13, and multiplied (Fig. 6) with tap coefficients.

Pertaining to the highlighted limitation "reception signal at predetermined intervals of n samples", Kokuryo discloses "the input signal vectors obtained by setting the input signals It and Qt in a time domain for respective delay times of the delay elements 2024 are represented by It and Qt". (paragraph 0090) Kokuryo indicates the Ir or It and Qr or Qt comprise of samples, which are produced by the analog to digital converter as shown in Fig. 1, label 3, within a

predetermined interval, since the term "vector" indicates multiple samples within a range.

The tap coefficients are determined based on the error, labels EI and Eq, and the symbol patterns, output from label 12. The errors, label EI and Eq, are determined based on the output from the training signal generator and the output from the equalizer as shown in labels 17-3,17-1,17-3. As per the rejection sent in the office action mailed 10/17/2006, Kokuryo fails to disclose updating the weights or tap coefficients based on the detection signals. Adireddy et al discloses inputting the received signal (Fig. 3, output from label 320) into the adaptive algorithm for updating weights (Fig. 3, label 335), wherein the weights are received by the equalizer (Fig. 3, label 325). Motivation is as stated in the office action mailed 10/17/2006.

Based on the above rebuttal, the rejection as stated in the office action mailed 10/17/2006 stands as stated. A copy is provided below.

4. On page 14, the applicant contends Kokuryo fails to disclose "at least the equalizing means of the claimed invention", more specifically the claimed limitation "reception signal at predetermined intervals of n samples".

The examiner respectfully disagrees. As per the rebuttal above, paragraph 0090 discloses "the input signal vectors obtained by setting the input signals It and Qt in a time domain for respective delay times of the delay elements 2021 are represented by It and Qt". The input signal vectors indicates "predetermined intervals of n samples" since the input signal is made up of plurality of samples (Fig. 14, output from label 3) and a vector indicates a plurality of samples within some range. Kokuryo further discloses the relation between input signal vectors and tap coefficient vectors Cbi and Cbq is determined. (paragraph 0090) This indicates the equalizer is multiplying the predetermined intervals of n samples or input signal vectors with the tap coefficients.

5. On page 15, the applicant contends Kokuryo in view of Adireddy fails to discloses "weight updating means for updating said weights based on said detection signal and said equalization error at the timing of said symbol patterns detected from said reception signal of the oversampling rate."

The examiner respectfully disagrees. Kokuryo discloses in Fig. 2, labels 12 and 15 the tap coefficient updating means updates the weights depending on the symbol pattern synchronization means or training signal synchronization detector. The equalization error is determined based on the generated training signal or symbol pattern as outputted by label 18, which depends on label 12. Label 12, outputs training signals or symbol patterns determined based on the sampled

signals, Ir and Qr. (labels Ir,Qr and 3) Since Ir and Qr are produced at a rate depending on the analog to digital converter, label 3, and the training signal synchronization detector determines the training signal depending on Ir and Qr, the training signals would comprise components such as timing and pattern, depending on the sampled Ir and Qr. Since oversampling is conventional as stated in the applicant's arguments, the analog to digital converter can perform oversampling so to produce oversampled Ir and Qr. The symbol patterns or training signals detected by label 12 would be from oversampled Ir and Qr as per the claimed limitations. As per the rejection stated in the office action mailed 10/17/2006, Adireddy discloses "weight updating means for updating said weights based on said detection signal". Please review the office action for the further explanation and motivation.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1,2** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kokuryo et al (US Patent No.: 20030165191) in view of Adireddy et al (US Patent No.: 6912250).

   a. **Claim 1**, Kokuryo et al discloses

   - symbol pattern synchronizing means (Fig. 12, label 12) for reproducing symbol timing by detecting said symbol patterns (page 5, paragraph 0085) based on said reception signal (Fig. 12, input to label 1);
   - equalizing means (Fig. 12, label 14) for acquiring an equalized signal by multiplying signals extracted from said reception signal at predetermined intervals of n samples and weights (paragraphs 0123-0146 , Fig. 6);
   - symbol pattern generating means (Fig. 12, label 18) for generating a reference signal at the same timing as the preamble detected by the timing signal synchronization detector (Fig. 12, labels 12,18);
   - error calculating means (Fig. 12, labels 17-3,17-1, EI and Eq) for acquiring an equalization error by subtracting (Fig. 12, labels 17-1,17-3) said equalized signal (Fig. 12, output from label 14) from said reference signal;
   - weight updating means (Fig. 12, label 15) for updating said weights based on said equalization error (Fig. 12, labels EI and Eq) at the timing of said symbol patterns (Fig. 12, output from label 12), wherein the symbol patterns are produced dependent on Ir and Qr (Fig. 12, labels Ir,Qr). Thus, the symbol patterns are detected from the reception signal, Ir, Qr, sampled at the rate as set by the digital to analog converter, label 3.

- Although Kokuryo et al fails to disclose sampling at an oversampling rate, it would be obvious to one skilled in the art to oversample depending on the rate set for the analog to digital converter as shown in Fig. 12, label 3 and to aid in anti-aliasing and producing digital signals.
- Although Kokuryo et al fails to disclose producing a weight update based on the detection signals, Adireddy et al discloses inputting the received signal (Fig. 3, output from label 320) into the adaptive algorithm for updating weights (Fig. 3, label 335), wherein the weights are received by the equalizer (Fig. 3, label 325). It would be obvious to one skilled in the art to incorporate using received signals in determining the weights inputted in the equalizer as disclosed by Adireddy et al into Kokuryo et al's invention to maximize "the performance of receivers that contain decision feedback equalizer capable of reducing precursor ISI." (Col. 2, lines 50-52)

b. **Claim 2**, Kokuryo et al discloses using QAM as a demodulation scheme (paragraph 0022). Although Kokuryo et al discloses using 16QAM as an example, 4QAM or any type of demodulation scheme with less than 4 symbols for QAM mapping are well known and it would be obvious to one skilled in the art to use such schemes based on design choice. Kokuryo et al discloses using least mean square method for updating taps. (paragraph 0029)

7. **Claims 3,5,7,9,13-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishikawa et al (US Patent No.: 5455844) in view of Kokuryo et al (US Patent No.: 20030165191), and further in view of Adireddy et al (US Patent No.: 6912250).

   c. **Claim 3** inherits all the limitations of claim 1, but claim 1 does not recite the limitations of a plurality of antennas, a plurality of detecting means, a plurality of equalizers, a selecting means and data decision means. Ishikawa et al discloses a plurality of antennas (Fig. 1, labels 11 and 21), a plurality of detecting means (Fig. 1, labels 12 and 22), wherein the training or known symbols are determined (Col. 2, lines 60-63), a plurality of equalizers (Fig. 1, labels 14,101,25,201) for carrying out equalization using the outputs of the corresponding receiving circuit (Fig. 1, labels 12 and 22), selecting means (Fig. 1, label 33) for selecting an output of the equalizers (Fig. 1, labels 18 and 28) and data decision means (Fig. 1, label 34 decision data sequence). As per the new limitations, Kokuryo discloses the equalizer determines the output based on the symbol pattern timing (Fig. 12, label 12), wherein the symbol patterns are produced from the reception signal, Ir, Qr, at the rate of the analog to digital converter, label 3. It would be obvious to one skilled in the art to incorporate Kokuryo et al and Adireddy et al's invention into Ishikawa et al's invention to improve receiving performance.

d. **Claim 5** inherits all the limitations of claims 1 and 3 but claims 1 and 3 fails to recite the limitation of a plurality of weight updating means, combining means for combining the output from the equalizers and error calculating means. Ishikawa et al discloses a plurality of weight updating means (Fig. 1, labels 201 and 101), combining the outputs (Fig. 1, labels 16,26,31) and error calculating based on the combined output (Fig. 1, labels 34,201 and 101) It would be obvious to one skilled in the art to incorporate Kokuryo et al and Adireddy et al's invention into Ishikawa et al's invention to improve receiving performance.

e. **Claim 7**, Kokuryo et al also discloses "As the training signal is received and this is detected by the training signal synchronization detector 12, the switches 16-3' are turned to the contact b side to suplly the detection signal to a tap coefficient updating unit 15 to start changing the equalization characteristics in the manner described above." (paragraph 0027) When the training signal is stopped, the switches are turned up and equalization is stopped. (paragraph 0041)

f. **Claim 9** inherits all the limitations of claims 1 and 3.

g. **Claim 13** inherits all the limitations of claims 3 and 7.

h. **Claim 14** inherits all the limitations of claim 2.

i. **Claim 15**, Kokuryo et al discloses a first, second, and third complex weight multiplier unit (Fig. 6, label 2022), an adder unit (Fig. 6, label 2023), wherein the adder unit outputs a result of adding up signals output from the first, second and third complex weight multiplier unit (Fig. 6, labels 2022 and 2023), wherein the equalization output would inherently be as stated in the limitations of claim 15

since the signal input is delayed and multiplied with the coefficients or weights, C1-CN.

j. **Claim 16**, Kokuryo et al disclose a first and second n sample delay unit (Fig. 6, label 2021), the first n sample delay unit outputs a first signal to the second n sample delay unit and the second complex weight multiplier (Fig. 1, labels 2021 and 2022) and wherein the second n-sample delay unit outputs a second signal to the third complex weight multiplier (Fig. 6, labels 2021 and 2022).

k. **Claim 17,** Kokuryo et al discloses a first and a second n-sample delay unit (Fig. 6, label 2021), a first, a second, and a third complex weight multiplier unit (Fig. 6, labels 2021,2022,c1-c3) and an adder unit (Fig. 6, label 2023), wherein said first n-sample delay unit (Fig. 6, label 2021) outputs a first signal to the second n-sample delay unit (Fig. 6, label 2021) and the second complex weight multiplier (Fig. 6, labels 2022 and c2), wherein said second n-sample delay unit (Fig. 6, label 2021) outputs a second signal to the third complex weight multiplier unit (Fig. 6, labels c3 and 2022), wherein the first complex weight multiplier (Fig. 6, label 2021) outputs a third signal to the adder unit (Fig. 6, label 2023), wherein the second complex weight multiplier (Fig. 6, label 2022 and c2) outputs a fourth signal to the adder (Fig. 6, output to label 2023) wherein the third complex weight multiplier (Fig. 6, label 2022 and c3) outputs a fifth signal to the adder unit(Fig. 6, output to label 2023), wherein the adder unit outputs a result of adding up the third signal, and the fourth signal, and the fifth signal output from the first, the second, and the third complex weight multipliers

as an equalization output G(t) (Fig. 6, labels 2023,2021,2022) to a data decision circuit and a subtracter unit (Fig. 12, labels 17-1), and wherein Kokuryo et al inherently disclsoes the equalization output G(t) is expressed by: G(t)=W0 • R(t)+W1 • R(t-nT) + W2o R(t-2nT). Regarding the limitation "said first n-sample delay unit and said multiplier unit receive as input said reception signal", Fig. 6 shows the first multiplier and label 2021 receiving the reception signal.

l. **Claim 18** inherits all the limitations of claim 17.

m. **Claim 19**, Kokuryo et al discloses outputing a value closest to the equalization output G(t) (Fig. 6) of a transmission QAM symbol mapping values (paragraph 0022) as demodulated data (Fig. 12, output from 16-2) at a symbol timing from a frame/symbol synchronization circuit (Fig. 12, label 12).

n. **Claim 20**, Kokuryo et al discloses 16QAM. (paragraph 0022)

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the

mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Linda Wong
3/16/2007

JAY K. PATEL
SUPERVISORY PATENT EXAMINER